CLAIMS

What is claimed is:

1. A method to correct a phase of a received phase modulated (PM) signal, comprising:

applying a received phase modulated (PM) signal to a first circuit branch and a second circuit branch;

in the first circuit branch, selecting k data bits from the received PM signal, wherein a data bit received most recently corresponds to time t_1 and wherein k is an integer greater than1;

determining a phase error based on the k data bits;

in the second circuit branch, delaying the PM signal to a second time t_2 that is later than t_1;

applying the phase error to at least a portion of the delayed PM signal at the second time t_2;

calculating a phase offset from the delayed PM signal; and

using the phase offset to correct phase of a PM signal received at a time later than t_1.

2. The method of claim 1 wherein selecting k data bits comprises arranging the k data bits serially so as to alternate between in-phase and quadrature bits.

3. The method of claim 1 further comprising:

setting k equal to a total number of data bits that influence the phase of the received PM signal at the first time t_1.

4. The method of claim 1 wherein $k=1+\frac{1}{BT}$, wherein B is a bandwidth of the received signal and T is a bit interval of the received signal.

5. The method of claim 1 wherein determining a phase error includes accessing, using the k data bits, a lookup table.

6. The method of claim 5 wherein determining a phase error further comprises inverting an output of the lookup table when the most recent data bit is one of an in-phase or a quadrature data bit.

7. The method of claim 1 wherein determining a phase error based on the k data bits comprises correlating the k data bits except the most recent data bit with a derivative with respect to phase of a conjugate of a reconstructed waveform.

8. The method of claim 7 wherein the derivative with respect to phase is stored in a lookup table.

9. A circuit to correct a phase of a phase modulated (PM) signal, comprising:

a first circuit branch wherein a primary phase shifter, a register, one of an algorithm sub-circuit and a lookup table sub-circuit, and a loop phase shifter are arranged in electrical series, in that order;

a second circuit branch having an input in parallel with the first circuit branch, wherein a delay block and the loop phase shifter are arranged in electrical series, in that order;

the register for storing at least two data bits sampled from the PM signal; and

the loop phase shifter having an output coupled to an input of the primary phase shifter.

10. The circuit of claim 9 wherein the at least two data bits comprises a series that alternates between an in-phase bit and a quadrature bit.

11. The circuit of claim 10 wherein the first circuit branch further comprises a complimentor block disposed between the loop phase shifter and the one of an algorithm sub-circuit and a lookup table sub-circuit.

12. The circuit of claim 9 wherein the at least two data bits comprises $k=n(1+\frac{1}{BT})$ data bits, wherein n is a number of samples per bit interval that is greater than or equal to one, B is a bandwidth of the received signal and T is a bit interval of the received signal.

13. The circuit of claim 9 wherein the one of the algorithm sub-circuit and the lookup table sub-circuit produces the phase correction by correlating all data bits in the register, except the most recent data bit, with a derivative with respect to phase of a conjugate of a waveform reconstructed from the received PM signal.